

## CMOS ANALOG MULTIPLEXERS/DEMULTIPLEXERS

### FEATURES

- ◆ Wide Range of Digital and Analog Signal Levels: Digital-3 to 15V, Analog-to 15V<sub>p-p</sub>
- ◆ Low ON-Resistance: 80Ω (typ.) over entire 15V<sub>p-p</sub> Signal-Input Range for V<sub>DD</sub>-V<sub>EE</sub> = 15V
- ◆ High OFF-Resistance: Input Leakage ± 10pA (typ) @ V<sub>DD</sub>-V<sub>EE</sub> = 10V
- ◆ Logic-Level Conversion for Digital Addressing Signals of 3 to 15V (V<sub>DD</sub>-V<sub>SS</sub> = 3V to 15V) to Switch Analog Signals to 15V<sub>p-p</sub> (V<sub>DD</sub>-V<sub>EE</sub> = 15V)
- ◆ Matched Switch Characteristics: ΔR<sub>ON</sub> = 5Ω (typ.) for V<sub>DD</sub>-V<sub>EE</sub> = 18V
- ◆ Very Low Quiescent Power Dissipation under all Digital Control Input and Supply Conditions: 1μW typ. @ V<sub>DD</sub>-V<sub>SS</sub> = V<sub>DD</sub>-V<sub>EE</sub> = 10V
- ◆ Binary Address Decoding on Chip

### DESCRIPTION

The 4051B, 4052B, and 4053B are Digitally-Controlled Analog Switches having low ON-impedance and very low OFF leakage current. Control of analog signals up to 15V<sub>p-p</sub> can be achieved by digital signal amplitudes of 3 to 15V. For example, if V<sub>DD</sub> = +5V, V<sub>SS</sub> = 0V, and V<sub>EE</sub> = -5V, analog signals from -5V to +5V can be controlled by digital inputs of 0 to 5V. The multiplexer circuits dissipate extremely low quiescent power over the full V<sub>DD</sub> - V<sub>SS</sub> and V<sub>DD</sub> - V<sub>EE</sub> supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the Inhibit input terminal all channels are OFF.

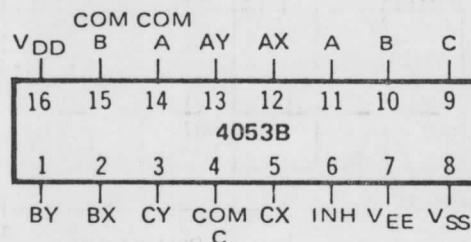
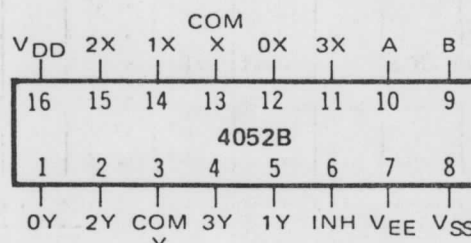
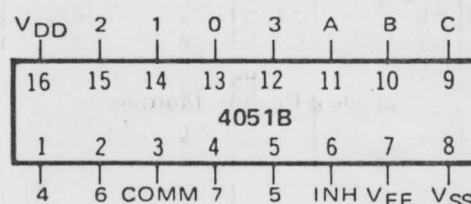
4051B is a Single 8-Channel Multiplexer having three binary Control inputs, A, B, and C, and an Inhibit input. The three binary signals select 1 of 8 channels to be turned ON and connect the input to the output.

4052B is a Differential 4-Channel Multiplexer having two binary Control inputs, A and B, and an Inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

4053B is a Triple 4-Channel Multiplexer having three separate digital Control inputs, A, B, and C and an Inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

When the devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminal(s) is (are) the input(s).

### CONNECTION DIAGRAMS (all packages)



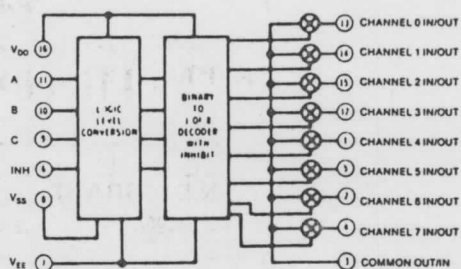
### RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

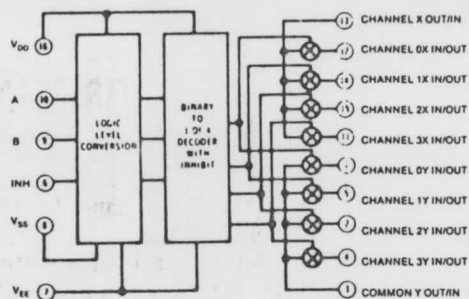
DC Supply Voltage	V <sub>DD</sub> - V <sub>SS</sub>	3 to 15	V <sub>dc</sub>
	V <sub>DD</sub> - V <sub>EE</sub>	3 to 15	V <sub>dc</sub>
Operating Temperature	T <sub>A</sub>		
C, D, F, H Device		-55 to +125	°C
E Device		-40 to +85	°C

NOTE: There are no restrictions on the relative magnitudes of V<sub>SS</sub> and V<sub>EE</sub>, providing Absolute Maximum Ratings are observed.

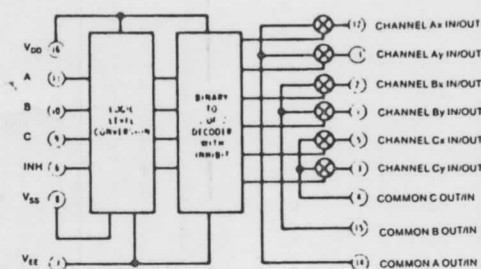
## LOGIC DIAGRAMS



**4051B**  
Single 8-Channel Multiplexer



**4052B**  
Differential 4-Channel Multiplexer



**4053B**  
Triple 2-Channel Multiplexer

## TRUTH TABLE

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	4051	4052	4053
0	0	0	0	0	Ox, Oy	cx, bx, ax
0	0	0	1	1	1x, 1y	cx, bx, ay
0	0	1	0	2	2x, 2y	cx, by, ax
0	0	1	1	3	3x, 3y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

\* = Don't care

## ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS<sup>1</sup>

PARAMETER	CONDITIONS	V <sub>SS</sub> (Vdc)	V <sub>DD</sub> (Vdc)	V <sub>EE</sub> (Vdc)	T <sub>LOW</sub> <sup>2</sup>		+25°C			T <sub>HIGH</sub> <sup>2</sup>		Units
					Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I <sub>DD</sub> V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DD</sub> All valid input combinations	0	+5	0	—	5	—	0.05	5	—	150	μAdc
		0	+10	0	—	10	—	0.1	10	—	300	
			+5	-5								
		0	+15	0	—	20	—	0.2	20	—	600	
			+7.5	-7.5								
MINIMUM INPUT HIGH VOLTAGE (Control and Inhibit Inputs)	V <sub>IH</sub> V <sub>IS</sub> =V <sub>EE</sub> V <sub>OS</sub> =V <sub>DD</sub> I <sub>OS</sub> =10μA	0	5	0	—	3.5	—	2.75	3.5	—	3.5	Vdc
		0	10	0	—	7.0	—	5.5	7.0	—	7.0	
		0	15	0	—	11.0	—	8.25	11.0	—	11.0	
MAXIMUM INPUT LOW VOLTAGE (Control and Inhibit Inputs)	V <sub>IL</sub> V <sub>IS</sub> =V <sub>EE</sub> V <sub>OS</sub> =V <sub>DD</sub> I <sub>OS</sub> =10μA	0	5	0	1.5	—	1.5	2.25	—	1.5	—	Vdc
		0	10	0	3.0	—	3.0	4.5	—	3.0	—	
		0	15	0	4.0	—	4.0	6.75	—	4.0	—	
SWITCH INPUT/ OUTPUT LEAKAGE Any channel OFF  All channels OFF	I <sub>OFF</sub> V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DD</sub> V <sub>IS</sub> =±7.5Vdc	0	+7.5	-7.5	—	±100	—	±0.01	±100	—	±1000	nAdc
	I <sub>OFF</sub> I <sub>IN</sub> =7.5Vdc V <sub>IS</sub> =±7.5Vdc	0	+7.5	-7.5								nAdc
					—	±400	—	±0.08	±400	—	±1000	
					—	±200	—	±0.04	±200	—	±1000	
ON-RESISTANCE	R <sub>ON</sub> V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DD</sub> V <sub>EE</sub> ≤V <sub>IS</sub> ≤V <sub>DD</sub> R <sub>L</sub> =10kΩ	-7.5	+7.5	-7.5								Ω
		0	+15	0	—	220	—	125	280	—	400	
		-5	+5	-5	—	310	—	180	400	—	590	
		0	+10	0								
		-2.5	+2.5	-2.5	—	2000	—	470	2500	—	3500	
		0	+5	0								
ON-RESISTANCE MATCH (Same Package)	ΔR <sub>ON</sub> V <sub>IN</sub> =V <sub>SS</sub> or V <sub>DD</sub> V <sub>EE</sub> ≤V <sub>IS</sub> ≤V <sub>DD</sub> R <sub>L</sub> =10kΩ	-7.5	+7.5	-7.5	—	—	—	5	—	—	—	Ω
		0	+15	0	—	—	—	10	—	—	—	
		-5	+10	-5	—	—	—	10	—	—	—	
		0	+10	0								
		-2.5	+2.5	-2.5	—	—	—	50	—	—	—	
		0	+5	0								

NOTES: <sup>1</sup> Remaining Static Characteristics are listed under "4000B Series Family Specifications".

<sup>2</sup> In certain applications, the external load-resistor current may include both V<sub>DD</sub> and signal-line components. To avoid drawing V<sub>DD</sub> current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R<sub>ON</sub> values shown).

No V<sub>DD</sub> current will flow through R<sub>L</sub> if the switch current flows into terminals 2, 3, 9, or 10. Failure to observe this condition may result in distortion of the signal.

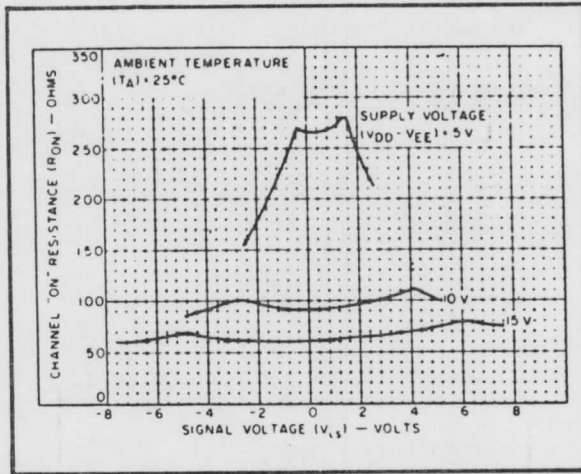
## ELECTRICAL CHARACTERISTICS (Continued)

DYNAMIC CHARACTERISTICS ( $C_L = 50\text{pF}$ ,  $T_A = 25^\circ\text{C}$ )

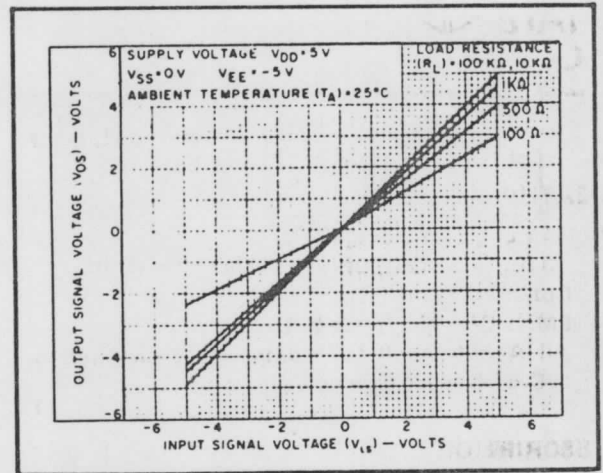
PARAMETER	CONDITIONS	$V_{SS}$ (Vdc)	$V_{DD}$ (Vdc)	$V_{EE}$ (Vdc)	Min.	Typ.	Max.	Units
SIGNAL INPUTS ( $V_{in}$ ) AND OUTPUTS ( $V_{os}$ )								
PROPAGATION DELAY TIME Signal Input to Signal Output	$t_{PLH}$ $t_{PHL}$ Inh = $V_{SS}$ $V_{IN} = V_{SS}$ or $V_{DD}$ $V_{in}$ = Square Wave $R_L = 10\text{k}\Omega$	0 0 0	5 10 15	0 0 0	— — —	30 15 12.5	60 30 25	ns
BANDWIDTH (-3dB) (Sine Wave)	BW Inh = $V_{SS}$ $V_{IN} = V_{SS}$ or $V_{DD}$ $V_{in} = 5V_{p-p}$ centered @ 0.0Vdc $R_L$ 1k $\Omega$ 10k $\Omega$ 100k $\Omega$ 1M $\Omega$	0	+5	-5	— — — —	54 40 38 37	— — — —	MHz
INSERTION LOSS ( $= 20 \log_{10} \frac{V_{os}}{V_{in}}$ )	Inh = $V_{SS}$ $V_{IN} = V_{SS}$ or $V_{DD}$ $V_{in} = 5V_{p-p}$ centered @ 0.0Vdc $R_L$ 1k $\Omega$ 10k $\Omega$ 100k $\Omega$ 1M $\Omega$	0	+5	-5	— — — —	2.3 0.2 0.1 0.05	— — — —	dB
SIGNAL DISTORTION (Sine Wave)	Inh = $V_{SS}$ $V_{IN} = V_{SS}$ or $V_{DD}$ $V_{in} = 5V_{p-p}$ centered @ 0.0Vdc $f_{in} = 1.0\text{kHz}$ $R_L = 10\text{k}\Omega$	-7.5 -5 -2.5	+7.5 +5 +2.5	-7.5 -5 -2.5	— — —	0.1 0.2 1.0	— — —	%
FEEDTHROUGH (-40dB)	Inh = $V_{SS}$ $V_{IN} = V_{SS}$ or $V_{DD}$ $V_{in} = 5V_{p-p}$ centered @ 0.0Vdc $R_L$ 1k $\Omega$ 10k $\Omega$ 100k $\Omega$ 1M $\Omega$	0	+5	-5	— — — —	1250 140 18 2	— — — —	kHz
CROSSTALK (-40dB) Between two switches	Inh = $V_{SS}$ $V_{IN} = V_{SS}$ or $V_{DD}$ $V_{in} = 5V_{p-p}$ centered @ 0.0Vdc $R_L = 1.0\text{k}\Omega$	0	+5	-5	—	1.0	—	MHz
CAPACITANCE Input	$C_{is}$ Inh = $V_{DD}$	0	+5	-5	—	5	—	pF
Common	$C_{os}$ 4051B 4052B 4053B	0	+5	-5	— — —	30 18 10	— — —	pF
Feedthrough	$C_{ios}$	0	+5	-5	—	0.2	—	pF
CONTROL INPUTS								
PROPAGATION DELAY TIME <sup>1</sup> Turn on	$t_{PLH}$ $t_{PHL}$ Inh = $V_{SS}$ $V_{EE} \leq V_{in} \leq V_{DD}$ $R_L = 10\text{k}\Omega$	0 0 0 0 -2.5 0	+7.5 +15 +5 +10 +2.5 +5	-7.5 0 -5 0 -2.5 0	— — — — — —	160 120 225 160 400 360	320 240 450 320 800 720	ns
INHIBIT INPUT								
PROPAGATION DELAY TIME Turn on	$t_{PLH}$ $t_{PHL}$ $V_{IN} = V_{SS}$ or $V_{DD}$ $V_{in} = V_{DD}$ $R_L = 10\text{k}\Omega$	0 0 0 0 -2.5 0	+7.5 +15 +5 +10 +2.5 +5	-7.5 0 -5 0 -2.5 0	— — — — — —	160 120 200 160 400 360	320 240 400 320 800 720	ns
INHIBIT RECOVERY TIME <sup>2</sup>	$t_{rel}$ $V_{IN} = V_{SS}$ or $V_{DD}$ $V_{EE} \leq V_{in} \leq V_{DD}$ $R_L = 10\text{k}\Omega$	0 0 0 0 -2.5 0	+7.5 +15 +5 +10 +2.5 +5	-7.5 0 -5 0 -2.5 0	— — — — — —	150 80 200 105 300 225	300 160 400 210 600 450	ns

Notes: <sup>1</sup> Channel Overlap time — interval following change of control input during which two channels may be ON simultaneously.<sup>2</sup> Interval following removal of Inhibit during which channel information is invalid.

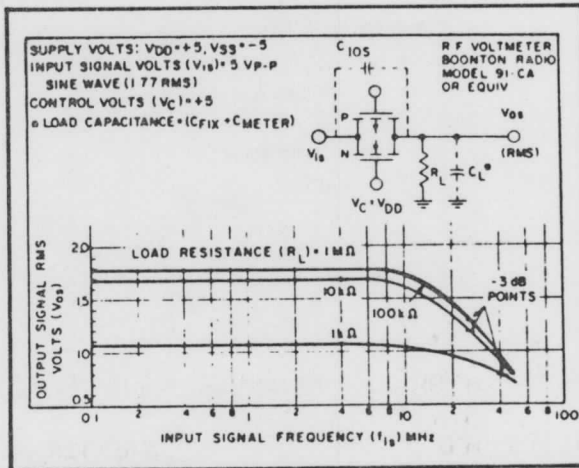




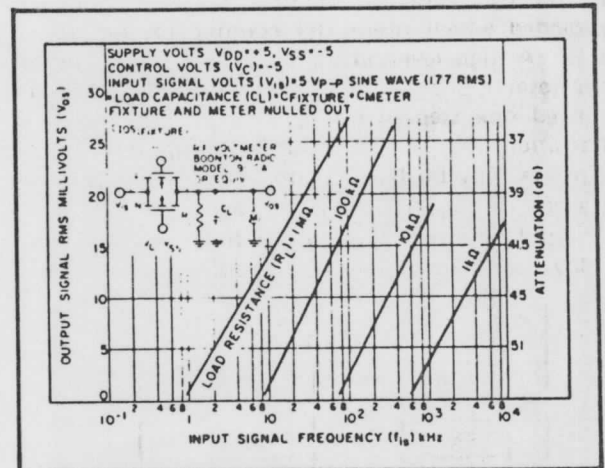
Typical Channel "ON" resistance vs. signal voltage



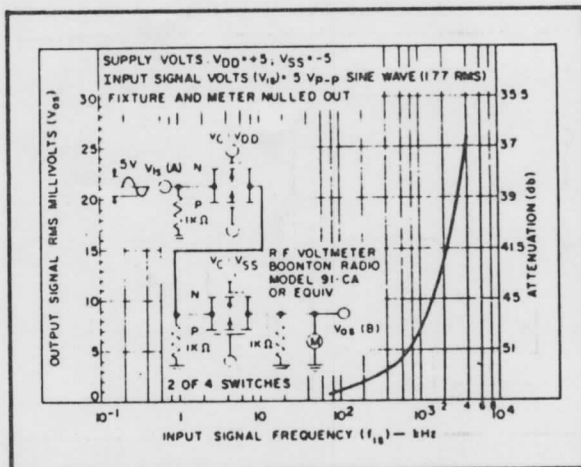
Typical "ON" characteristics



Typ. switch frequency response-switch "ON"



Typ. feedthru vs. freq. - switch "OFF"



Typ. crosstalk between switch circuits in the same package

# SCHEMATIC DIAGRAM OF ONE SWITCH

